

Attorney Docket No. C2397 COGG
Serial No. 10/075,726
Art Unit: 1743
Applicants' Response to the Office Action dated December 9, 2005

Amendments to the Claims

Please amend claims 1, 6, 9, 11, 13, 18, 19 and 20 and add new claims 21-30, as shown in the Listing of Claims below. The amendments add no new matter. This listing of claims is a complete listing of all claims ever presented in the application and replaces all prior versions, and listings, of the claims in the instant application:

Listing of Claims:

Claim 1 (Currently amended): A chip reactor comprising a carrier having at least two different geometric forms of integral microreaction channels, each of the channels comprising at least one reaction space, at least one inlet for one or more reaction educts, and at least one outlet for one or more reaction products, wherein each of the two or more of the at least two different geometric forms of integral microreaction channels is are suitable for operation independently of the one another.

Claim 2 (Original): The chip reactor according to claim 1, wherein the carrier comprises a silicon/glass composite.

Claim 3 (Currently amended): The chip reactor according to claim 2, wherein at least a portion of the channels at least one microreaction channel is etched.

Claim 4 (Original): The chip reactor according to claim 2, wherein at least a portion of the at least one reaction space is coated with silicon dioxide.

Claim 5 (Original): The chip reactor according to claim 4, wherein the silicon dioxide has a thickness of from 50 to 2000 nm.

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Claim 6 (Currently amended): The chip reactor according to claim 1, wherein the carrier has from 2 to 100 different geometric forms of integral microreaction channels, ~~each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independently of the other.~~

Claim 7 (Previously presented): The chip reactor according to claim 1, wherein each of the reaction spaces comprises a channel having a length of from 1 to 500 mm.

Claim 8 (Currently amended): The chip reactor according to claim 1, wherein one or more of the reaction spaces have one or more mixing points.

Claim 9 (Currently amended): The chip reactor according to claim 1, wherein at least one of the microreaction channels has at least two inlets for at least two reaction educts, ~~the at least two inlets impinging on each other at a mixing angle of from 15° to 270°.~~

Claim 10 (Currently amended): The chip reactor according to claim ~~1~~ 2, wherein ~~at least one of the reaction spaces has one or more mixing points~~ the at least two inlets impinge on each other at a mixing angle of from 15° to 270°.

Claim 11 (Currently amended): The chip reactor according to claim 1, wherein at least a portion of the carrier ~~the chip reactor~~ is divided into two or more zones, comprising mixing, reaction, heating or cooling zones, for variable processing.

Claim 12 (Original): The chip reactor according to claim 11, wherein the two or more zones can be heated/cooled independently of one another.

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Claim 13 (Currently amended): The chip reactor according to claim 1, wherein the carrier is embedded in a manifold having ~~an~~ at least one inbound passageway ~~corresponding connected~~ to the at least one inlet and ~~an~~ at least one outbound passageway ~~corresponding connected~~ to the at least one outlet.

Claim 14 (Original): The chip reactor according to claim 13, wherein the manifold comprises an inert material.

Claim 15 (Currently amended): The chip reactor according to claim 13, wherein the manifold further comprises at least one passageway, in thermal contact with at least one microreaction channel, for a heat transfer liquid.

Claim 16 (Currently amended): The chip reactor according to claim 13, wherein the manifold further comprises a facility for visual inspection of at least a portion of the chip reactor.

Claim 17 (Original): The chip reactor according to claim 13, further comprising a seal separating the chip reactor from the manifold.

Claim 18 (Cancelled)

Claim 19 (Currently amended): The chip reactor according to claim 1, wherein the carrier has from 5 to 50 different geometric forms of microreaction channels, ~~each of the channels comprising at least one reaction space, at least one inlet and at least one outlet~~, wherein each of the different channels is suitable for operation independently of the other.

Claim 20 (Currently amended): A chip reactor comprising a silicon/glass composite carrier wafer having ~~from 5 to 50~~ at least two different geometric forms of integral microreaction

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channels etched therein, each of the microreaction channels comprising at least one reaction space, a portion of which is coated with silicon dioxide having a thickness of from 50 to 2000 nm, at least one inlet for one or more reaction educts and at least one outlet for one or more reaction products, wherein ~~each of~~ at least a portion of the microreaction channels ~~is~~ are suitable for operation independently of the other, and wherein the carrier is embedded in an inert manifold having an inbound passageway ~~corresponding~~ connected to each inlet, an outbound passageway ~~corresponding~~ connected to each outlet[,]] and at least one passageway for a heat transfer liquid ~~and a facility for visual inspection of the chip reactor.~~

Claim 21 (New): The chip reactor according to claim 20, wherein the at least a portion of the microreaction channels are divided into two or more mixing zones, two or more reaction zones, two or more mixing and reaction zones, two or more cooling or heating zones or any combinations thereof.

Claim 22 (New): The chip reactor according to claim 21, wherein the microreaction channels are divided into two reaction zones and one cooling zone.

Claim 23 (New): The chip reactor according to claim 20, wherein at least one of the reaction spaces has one or more mixing points.

Claim 24 (New): The chip reactor according to claim 20, wherein at least one of the microreaction channels has at least two inlets for at least two reaction educts.